PREPARING FOR THE NEXT WAVE OF HIGH SPEED FABRICS IN EMBEDDED COMPUTING

Embedded Tech Trends | Burrell Best | SI Architect

AGENDA

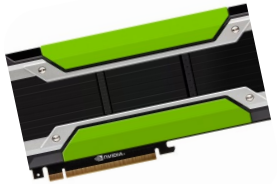
- Industry Trends Driving Technology
- Next Wave of High Speed Standards
- Impact on System Design
- Innovations in Interconnect Technologies with Examples
- Takeaways & Summary

INDUSTRY TRENDS DRIVING TECHNOLOGY

DATA GROWTH IS DRIVING THE INDUSTRY

Critical Business Need

Data needs to be analyzed quickly. The value of analyzed data decreases over time.

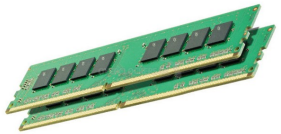


New Devices

FPGA and GPU based Accelerators are being used to "Accelerate" parallel computing workloads. This market is expected to jump to 21.1 B by 2023, from 2.84B currently. Fabric attached Storage, and NVMe connected SSDs.

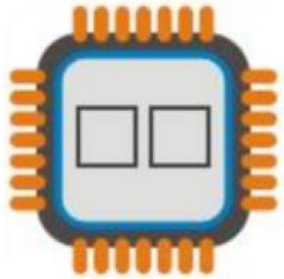
Data Intensive Workloads

Advances in Artificial Intelligence (AI) specifically in the areas of machine vision, machine learning, and advanced analytics are fueling growth.



Memory Technologies

New Phase Change Memory (PCM) technologies like 3D Crosspoint, co-developed by Intel & Micron, are making memory faster, denser, and non-volatile. This will also migrate into the Storage and DDR markets.



Embedded Compute Power

Moore's Law, multi-core processors, and advanced CPU power management designs continue to boost compute power. This is providing amazing performance per watt to embedded systems.

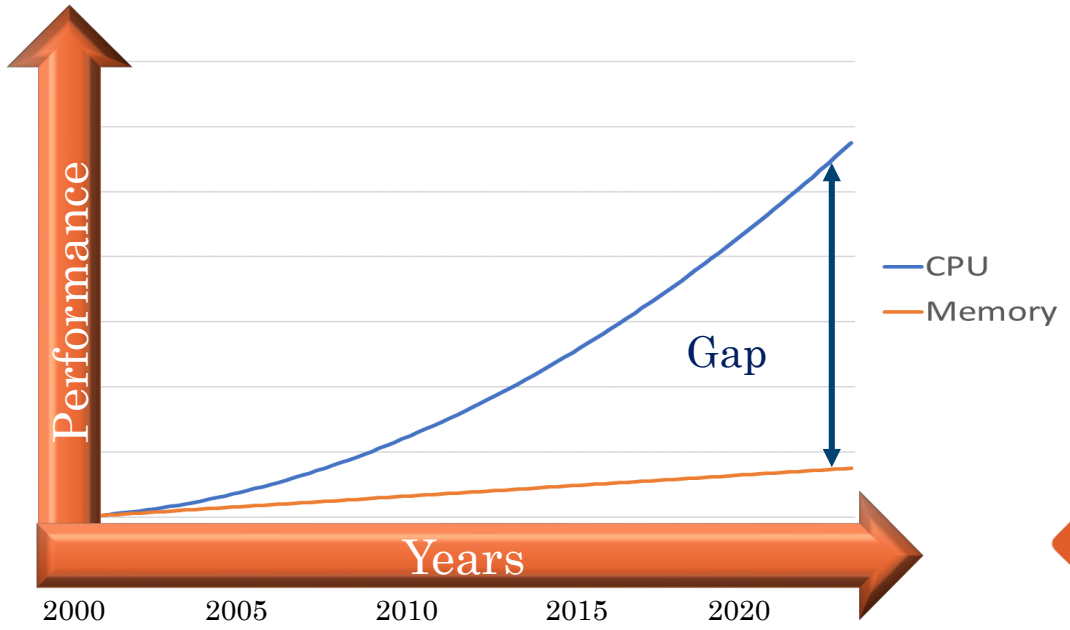
Fabric Technologies

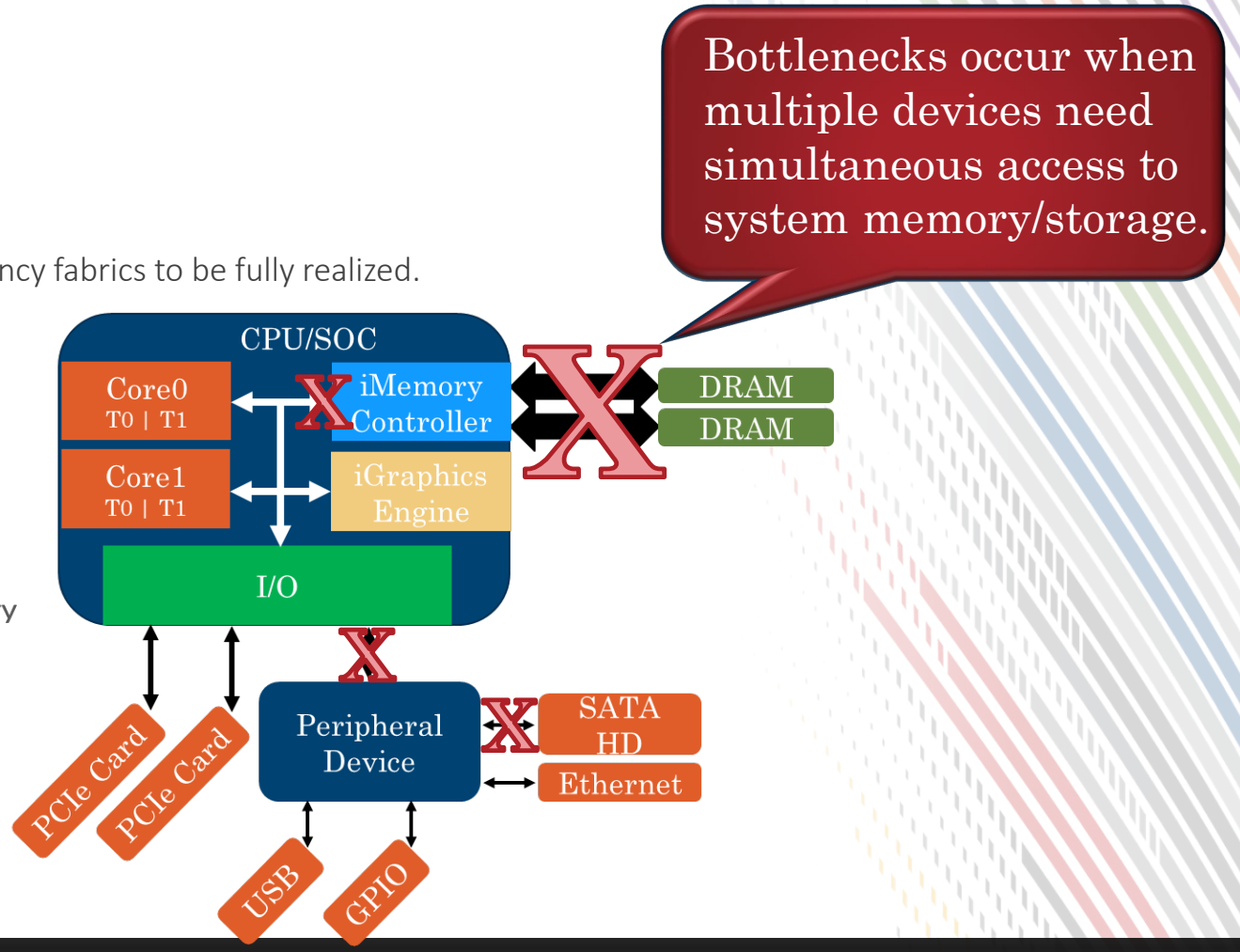
Ethernet and PCI Express bus speeds continue to increase. New fabric architectures like CCIX and Gen-Z are emerging as low latency alternatives to traditional I/O.

MOORE'S LAW EFFECT & THE VON NEUMANN BOTTLENECK

- The continuation of Moore's Law has exacerbated the Von Neumann Bottleneck.
  - Transistor density is still roughly doubling every ~18-24 months.
  - Single Threaded Performance/Watt continues to increase.
  - Number of logical cores continues to increase.

- Memory performance has not kept pace.
  - Performance gains due to new memory technologies need low latency fabrics to be fully realized.





NEXT WAVE OF HIGH SPEED STANDARDS

EMERGING STANDARDS

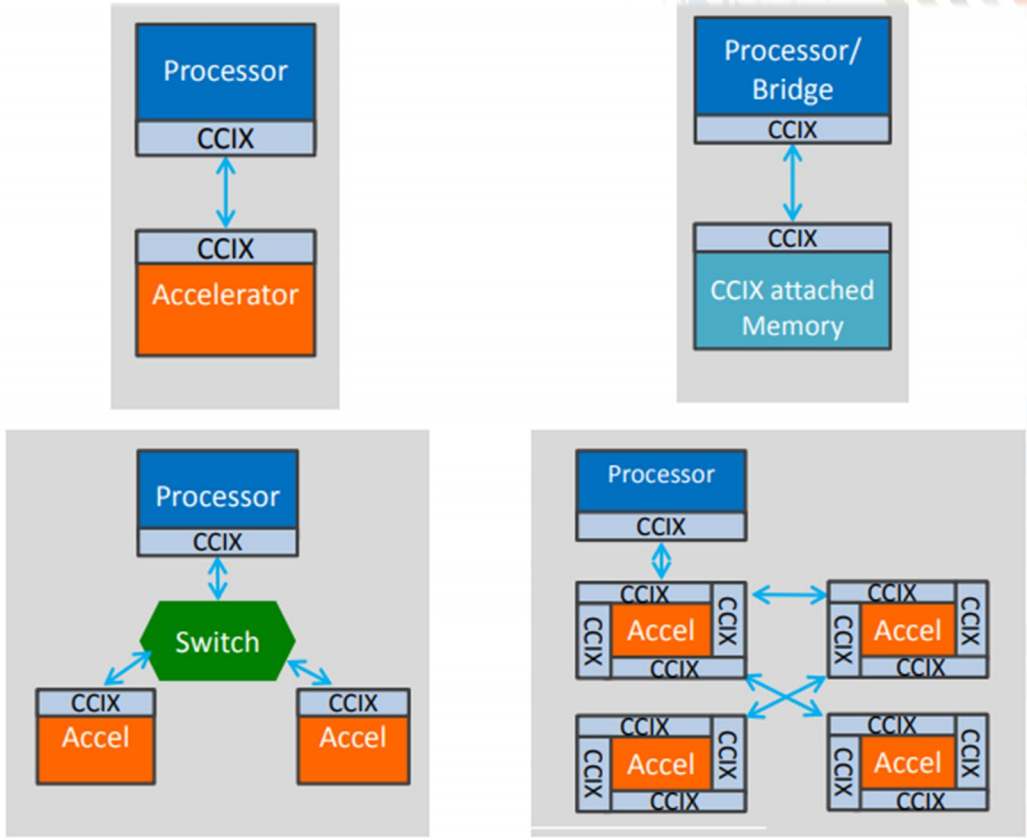
- New bus/fabric standards
  - **CCIX™ -** Cache Coherent Interconnect for Accelerators
  - **Gen-Z™**
- Motivation
  - Provide a low latency fabric to decrease the gap between processor and memory performance.
  - To provide standardized-open solutions.

Standard	Physical Layer	Topology	Signal Rates	Mechanicals	Coherence
CCIX	PCIe PHY	P2P & Switched	PCIE 4.0, 20GT/s, & 25GT/s	PCIe	Full Coherence between CPU and Accelerators
Gen-Z	IEEE 802.3 PHY 25BASE-SR/LR	P2P & Switched	PCIE 4.0, 25-28GT/s	SFF-TA-1002 (2.5G–56G NRZ, 112G PAM4)	Not natively coherent, but supports cache coherent protocols

CACHE COHERENT INTERCONNECT FOR ACCELERATORS

- Feature Highlights
  - Tightly coupled interface between processors, accelerators, and memory.
  - In the box solution.
  - Backwards compatible extension of PCI Express
- Use Cases
  - Allows low latency extension of main memory
  - Extends cache coherency to fabric attached devices and accelerators (GPUs,FPGAs).
- Physical Layer Roadmap

Current	Next	Future
PCIE 4.0 EDR-20G EDR-25G	PCIE 5.0	56G PAM4

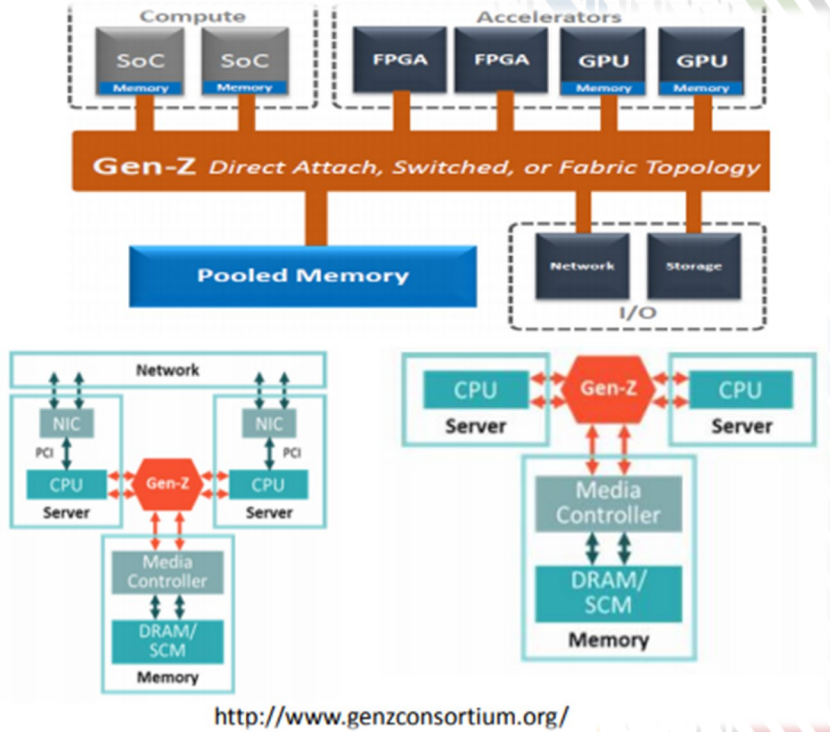


http://www.ccixconsortium.com/

GEN Z™

- Feature Highlights
  - Scalable - direct attach, switched, and fabric topologies.
  - Gateway to other networks
  - Multiple link widths, 1-256 lanes
  - Simplifies data access to memory operations (Byte addressable load/store, messaging, and IO block accesses)
  - PHY layer can run at PCI Express speeds
- Use Cases
  - General Purpose I/O
  - Fabric attached persistent memory
  - Single node and node to node interconnect
- Physical Layer Roadmap

Current	Next	Future
PCIE 4.0 25-28 Gbps	50-56G PAM4 PCIE 5.0	110-112G PAM4



http://www.genzconsortium.org/

samtec

EVOLVING STANDARDS

Optical Interface Forum

- **Current:** CEI-4.0, 6-56G NRZ, ENRZ and PAM4 channel definitions
- Future: CEI-5.0, Draft specs for 112G NRZ, CNRZ, PAM4 channels proposed – WIP.

Ethernet

- Current: 802.3cd – 50 Gb/s, 100 Gb/s, 200 Gb/s (PAM4). Signal rate 26.5625 Gb/s
- Future: 802.3ck – 100Gps, 200 Gb/s, 400 Gb/s (PAM4). Signal rate 50 Gb/s

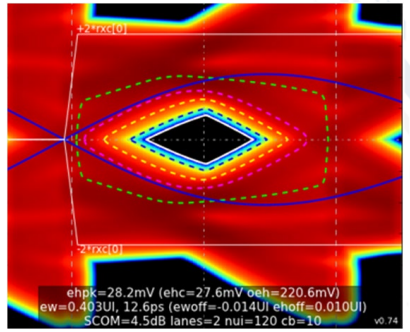
PCI Express

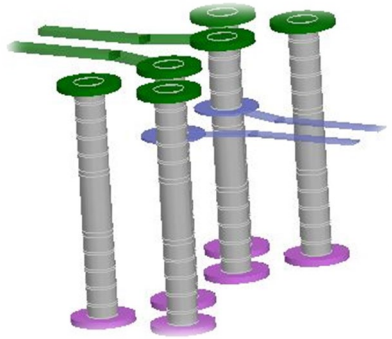
- Current: PCIe 4.0 – 16 GT/s
- Future: PCIe 5.0 – 32 GT/s

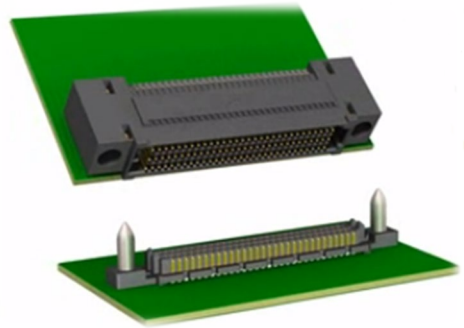
IMPACT ON SYSTEM DESIGN

SIGNAL INTEGRITY MATTERS!

- Simulation - Expertise in full computer aided design software and channel simulations will become critical.
  - Many real world channels traverse through non-standard connectors. For example, PCI Express over a mezzanine backplane connector.
- Routing - control via stubs to reduce reflections:
  - Use micro vias, via-in-pads, or back-drilling.
  - Break out high speed traces to layers that have the shortest via stubs
  - Limit the use of microstrip routing which may have higher loss due to X-talk.
- Other recommendations:
  - Consider optimizing the trace impedance to match the channel's interconnects, not necessarily the designed protocol impedance.
  - Manage differential skew.



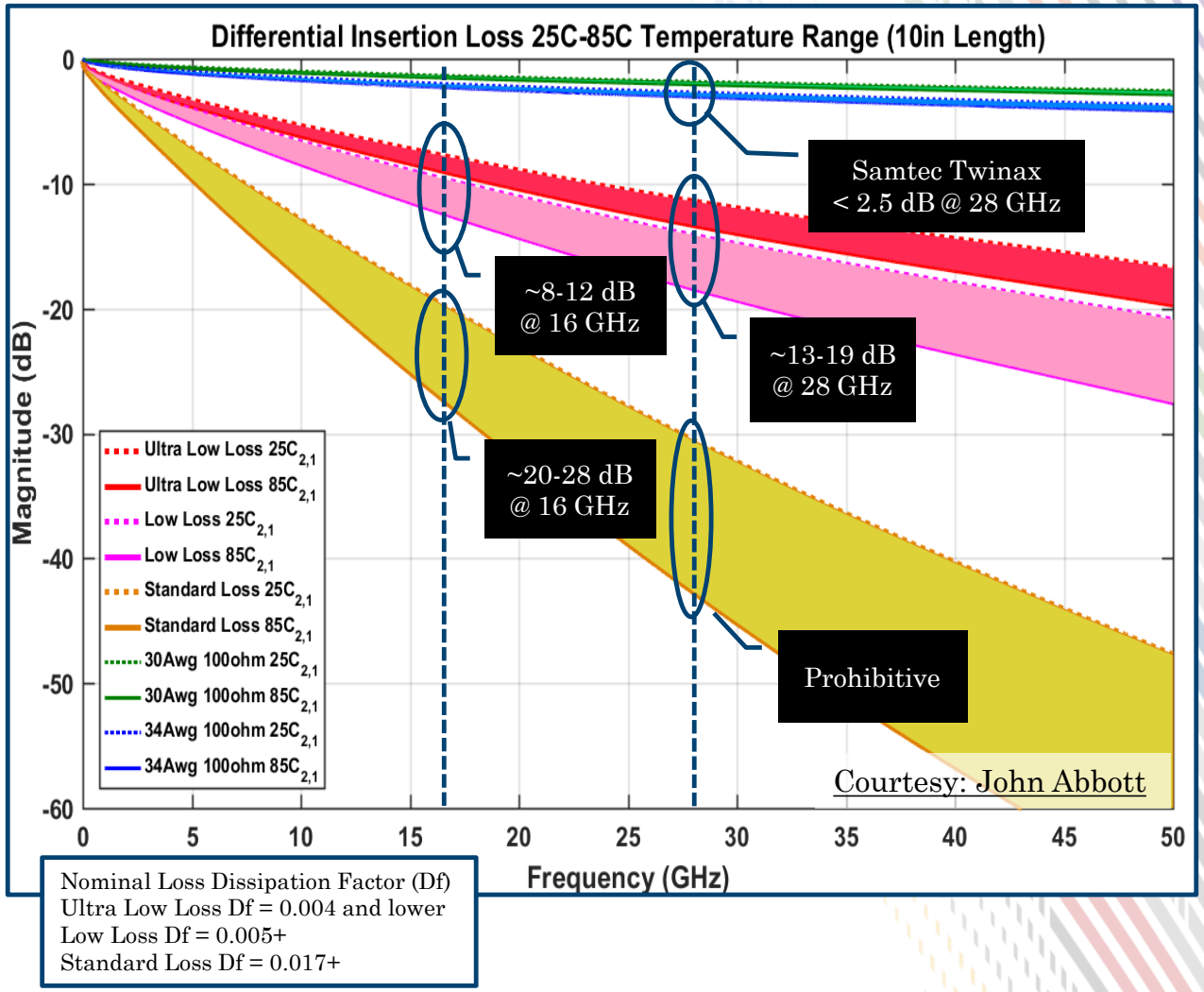




Courtesy: Steve Krooswyk

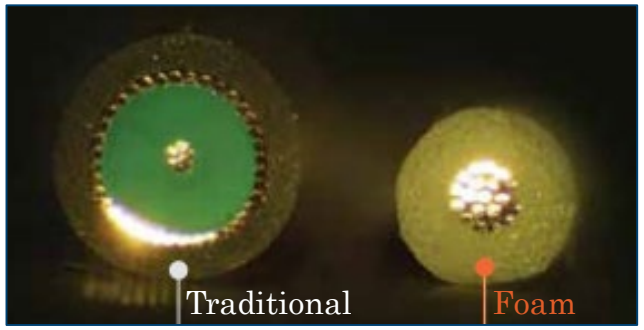
NEW CONSTRAINTS AS FR4 BECOMES PROHIBITIVE

- PCB materials:
  - Trending to ultra-low loss dielectrics
  - Target ~1 dB/inch at Nyquist.
  - Thermal environment has a larger impact on loss/inch.
- High speed cabling:
  - Trending to ultra thin gauge cable and low loss dielectrics .
  - Sophisticated manufacturing to control skew and improve loss.
  - Multiple termination options.
  - Superior SI performance over PCB materials.

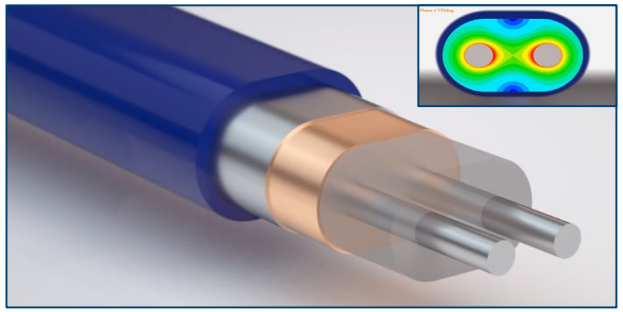


INNOVATIONS IN INTERCONNECT TECHNOLOGIES

INNOVATIONS IN COPPER CABLING



Foamed Fluorinated Ethylene Propylene (FEP) versus traditional solid dielectrics introduce air pockets to lower dielectric losses.



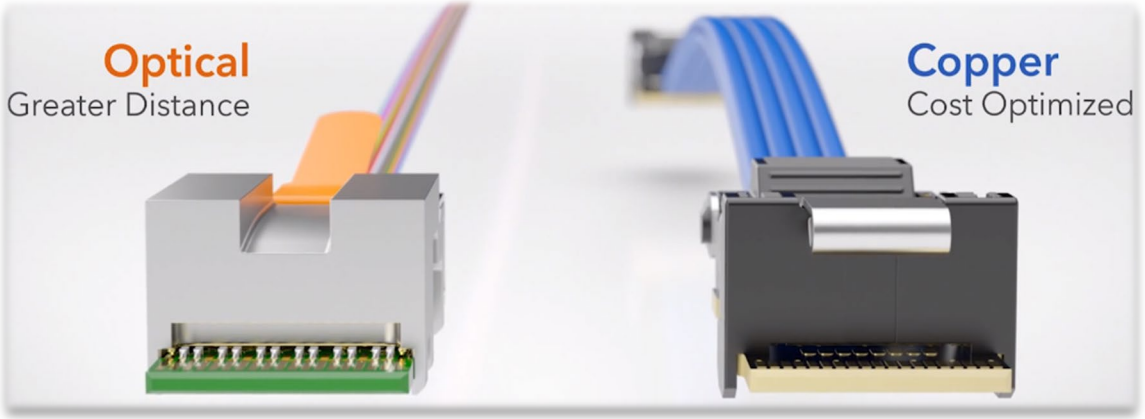
Sophisticated manufacturing processes like co-extrusion of dielectrics and conductors reduces loss by providing tighter coupling between conductors while almost eliminating differential skew.

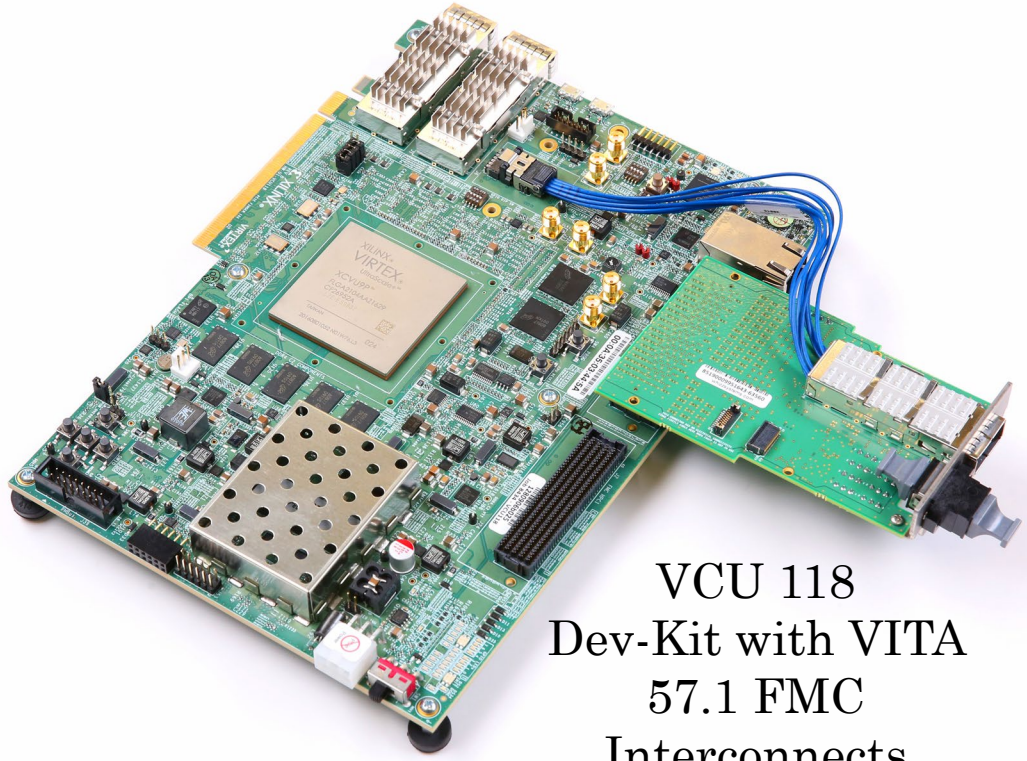
Direct attached cable terminations help reduce impedance mismatches and loss due to reflections.

FLYOVER CABLE EXAMPLE

FireFly™ Micro Flyover System™

- ❑ Data flies over lossy PCB up to 28Gbps
- ❑ Industry leading miniature footprint
- ❑ Multiple lanes - X4 and x12
- ❑ Copper and Optical interconnects are interchangeable
- ❑ Multiple high density rugged end2 options
- ❑ Extended Temperature FireFly™ with a -40 ºC to +85 ºC range for military and industrial applications (ETUO)
- ❑ Supports PCI Express

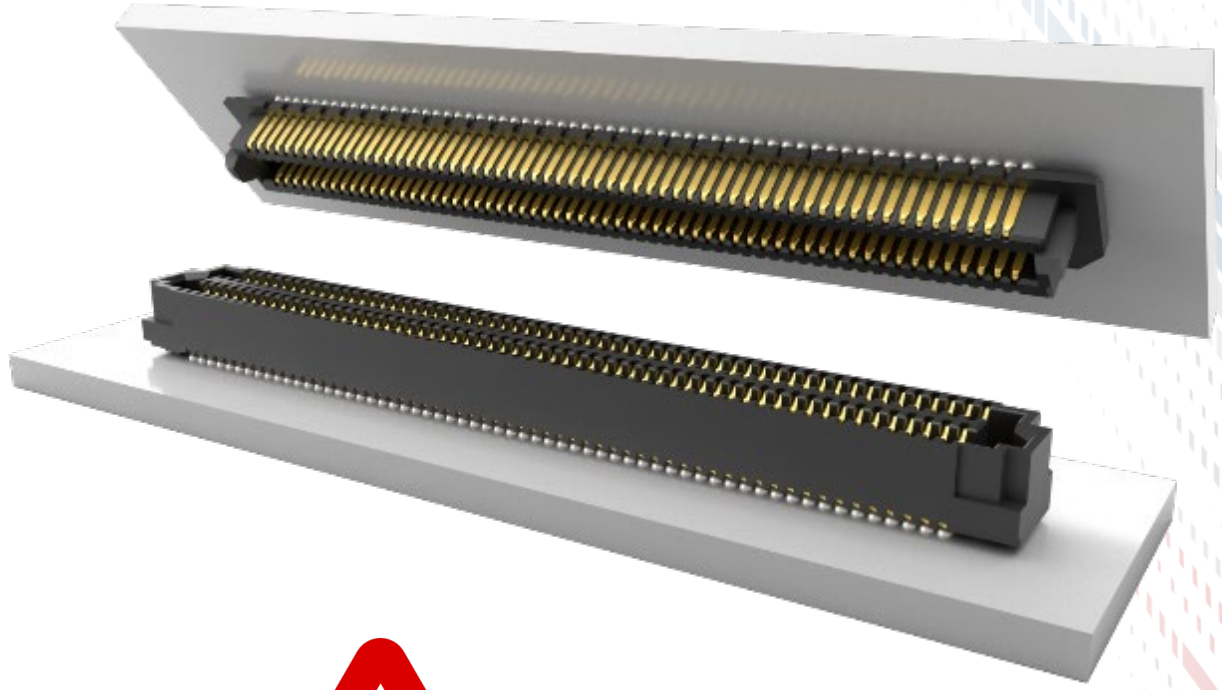




VCU 118
Dev-Kit with VITA
57.1 FMC
Interconnects

CONNECTOR TRENDS

- ✔ High Pin Count
- ✔ Density
- ✔ Performance

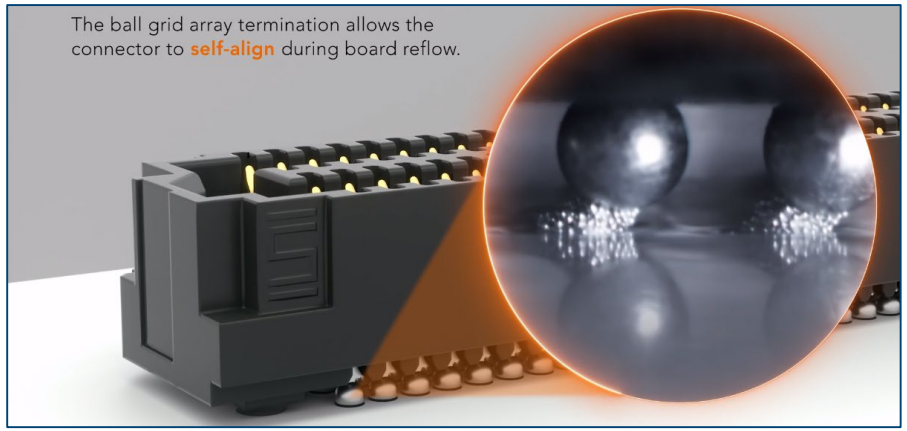


ADX6 Series (240 total positions)

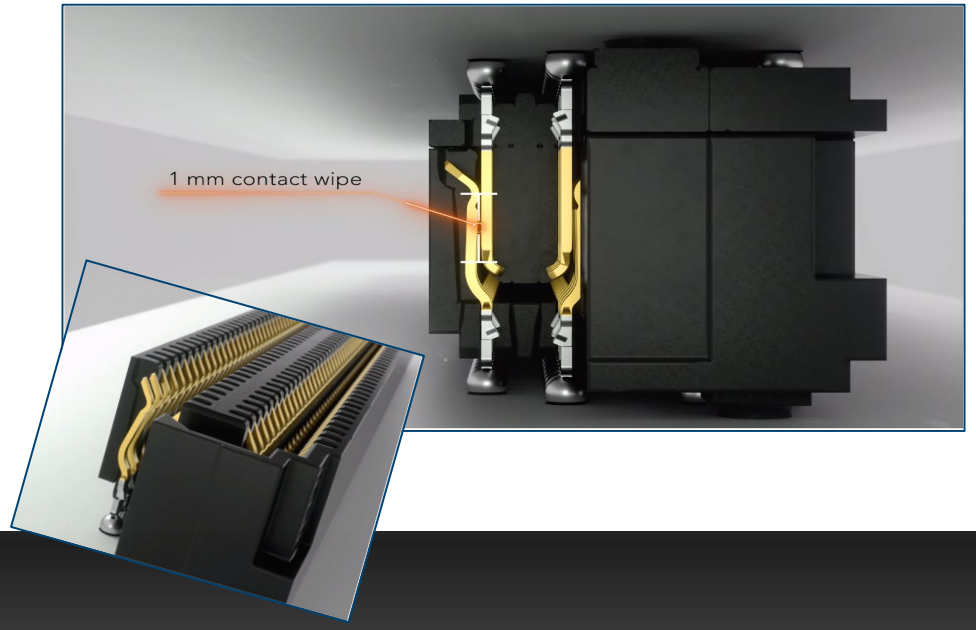
QXH Series (240 total positions)

What about crosstalk?

INNOVATIONS IN MEZZANINE CONNECTORS



Surface mount technology mitigates X-talk by reducing reflections associated with through-hole and press-fit designs. SMT eases BOR optimization and has the added benefit of self aligning during reflow.



Increased contact wipe combined with a narrow contact edge minimizes broadside coupling and reduces crosstalk. Also improves impedance continuity.

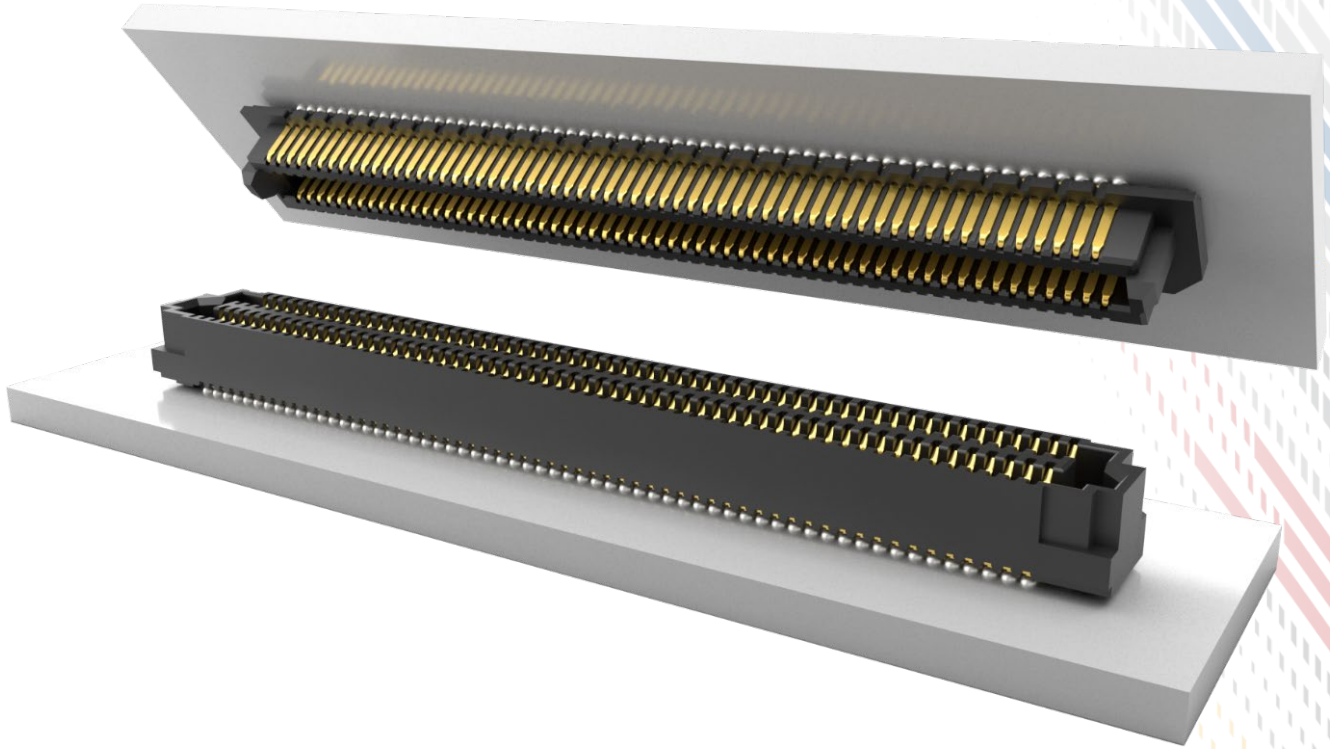
- Example - Edge Rate ® Contact Design

OPEN PIN FIELD CONNECTOR EXAMPLE

ACCELERATE® HD

BGA - Open pin field design

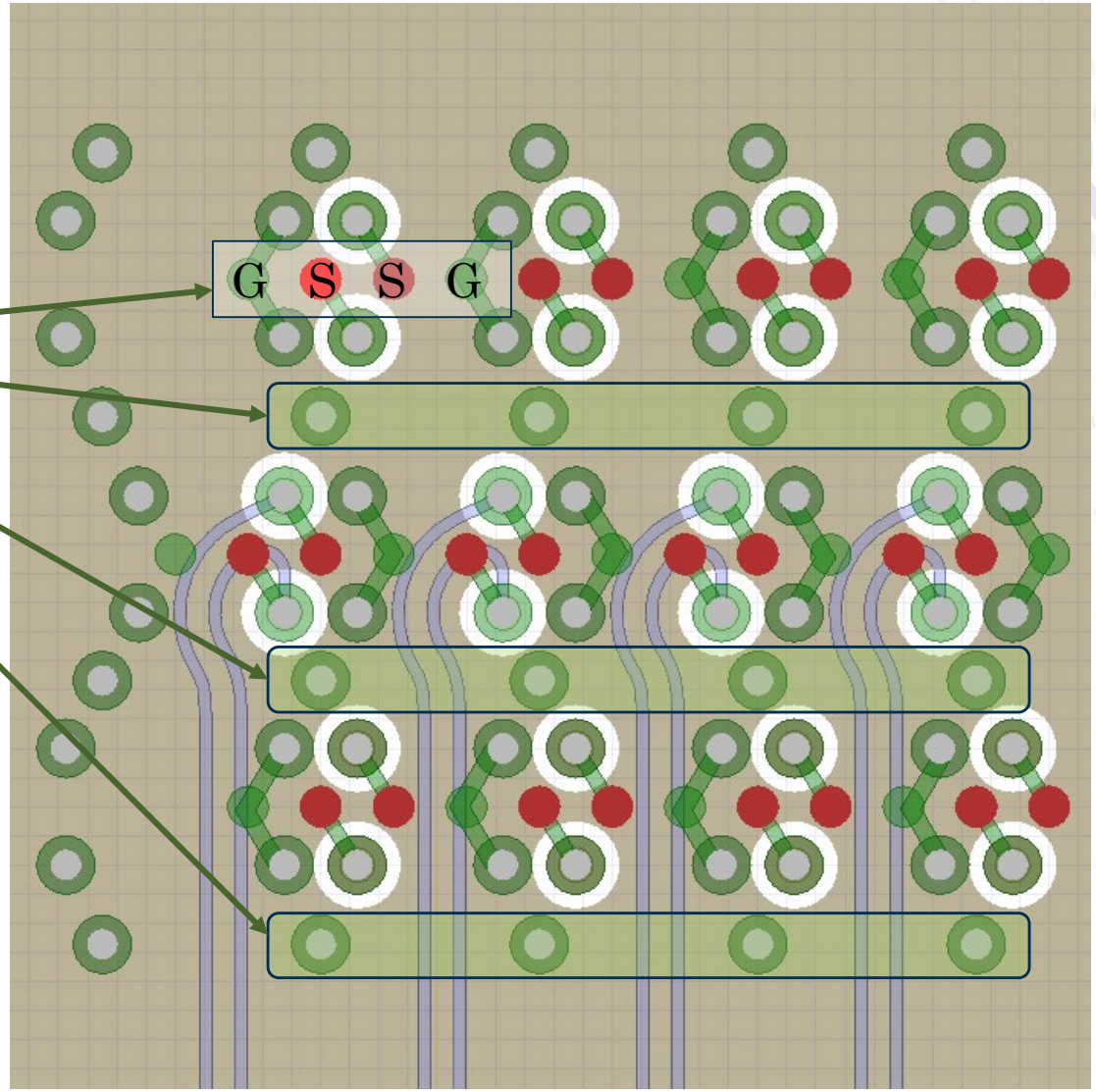
- Up to 260 positions (4 X 65)
- 2.2mm row-row pitch
- 0.635 mm pin pitch
- 5 & 10 mm stack height
- PCIE G5 Capable (32GTs)
- Ethernet 56 Gbps (PAM4)



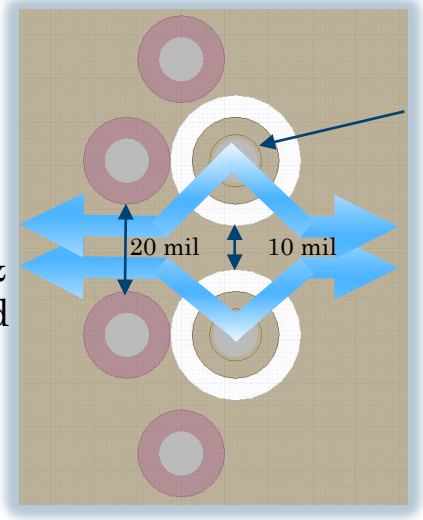
ACCELERATE®HD

Increased row to row spacing:

- ✔ Reduces Crosstalk
- ✔ Allows more Gnd VIAs
- ✔ Maintains density (GSSG)
- ✔ Eases differential routing



Bi-directional Routing



25 mil (.635 mm) pitch provides 20 mil pad-pad & 10 mil apad-apad spacing

TAKEAWAYS AND SUMMARY

- An explosion in the growth of data fueled by the Datacenter, AI, Autonomous Systems, etc. is driving technology forward.
- A new wave of next generation fabrics is being developed and standardized to process data faster, while overcoming the traditional memory bottlenecks that have stymied progress thus far.
- These next generation fabrics are promising incredible performance, but close attention to PCB materials, routing, BOR optimization, and interconnects will be critical to success.
- These next gen fabrics, and the technologies they enable, will have a huge impact on the embedded market.

THANK YOU

Burrell Best, SI Architect

Burrell.best@samtec.com

David Givens, Standards Director

David.givens@Samtec.com

StandardsISG@Samtec.com

Standards@Samtec.com